67,200-367
Serial Number 09/821,554

REMARKS

Favorable reconsideration of this application in light of the following remarks is respectfully requested.

Claims 1-15 are pending in this application. No claims are amended herein. No claims have been allowed.

Claim Rejections - 35 U.S.C. §§ 103

1. The Examiner has rejected claims 1-7 under 35 U.S.C. § 103(a) as being unpatentable over Yu et al. (U.S. Patent No. 6,004,883; hereinafter "Yu") in view of Hopper et al. (U.S. Patent No. 6,030,901; hereinafter "Hopper") and Avanzino et al. (U.S. Patent No,. 5,691,238; hereinafter "Avanzino").

2. The Examiner has rejected claims 8-15 under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino, and further in view of Chiang et al. (U.S. Patent No. 6,027,995; hereinafter "Chiang").

Applicant notes that Yu (as cited within paragraph 2, pages 2-3 of the Office communication mailed on 7 August 2002 and made FINAL) is cited as a base reference against which applicant's claims to applicant's invention are rejected. Hopper (as cited within page 4, second paragraph of the Office communication mailed on 7 October 2002 and made FINAL) is cited as disclosing various low dielectric constant dielectric materials. Avanzino (as cited within page 5, first paragraph of the Office communication mailed on 7 August 2002 and made FINAL)

is cited as disclosing anisotropic etching. Chiang (as cited within page 6, first paragraph of the Office communication mailed on 7 August 2002 and made FINAL) is cited as disclosing chemical mechanical polish (CMP) planarizing methods for forming patterned conductor layers.

In response applicant asserts that none of applicant's claims to applicant's invention may properly be rejected under 35 U.S.C. § 103(a) over either of the above combinations of references insofar as: (1) Hopper, when viewed in its entirety, clearly teaches away from that which is disclosed and claimed by applicant within claim 1 and claim 8 and thus may not properly be employed in rejecting any of applicant's claims to applicant's invention under 35 U.S.C. § 103(a); and (2) none of the remaining references as cited by the Examiner provides, for purposes of rejecting applicant's claims to applicant's invention under 35 U.S.C. § 103(a), the limitations for which Hopper is cited.

With respect to Hopper, applicant in particular notes that while the Examiner accurately cites Hopper at col. 2, lines 47-55 as disclosing a multiplicity of low dielectric constant dielectric materials for forming patterned low dielectric constant dielectric layers which may define dual damascene apertures which may be filled employing dual damascene methods, Hopper's dual damascene structure as illustrated in Fig. 2 apparently illustrates with respect to a dual damascene aperture a patterned dielectric layer formed of a single dielectric material rather than a laminated pair of dielectric material layers with intrinsic etch stop characteristics, as is required within applicant's invention as disclosed and claimed within claim 1 and claim 8. Thus, since applicant's dual damascene method as disclosed and claimed within claim 1 and claim 8 requires a laminated pair of dielectric material layers with intrinsic etch stop characteristics and Hopper discloses a dual damascene method clearly employing a single dielectric material layer

intrinsically, implicitly or inherently absent intrinsic etch stop characteristics, applicant asserts that Hopper in pertinent part, and when viewed in its entirely, teaches away from that which is disclosed and claimed by applicant. Thus, Hopper may not properly be employed in rejecting any of applicant's claims to applicant's invention under 35 U.S.C. § 103(a). MPEP 2141, 2141.02.

Since: (1) Hopper may not properly be employed in rejecting any of applicant's claims to applicant's invention under 35 U.S.C. § 103(a); and (2) none of the remaining prior art references as cited by the Examiner and employed in rejecting applicant's claims to applicant's invention alternatively provide the limitations for which Hopper was cited, applicant asserts that none of applicant's claims to applicant's invention may properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over either: (1) Yu in view of Hopper and Avanzino; or (2) Yu in view of Hopper and Avanzino, and further in view of Chiang.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of: (1) claims 1-7 under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino; and (2) claims 8-15 under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino, and further in view of Chiang, be withdrawn.

67,200-367
Serial Number 09/821,554

Response to Arguments

Applicant provides the foregoing alternative traversal to the Examiner's rejections of applicant's claims 1-7 or 8-15 under 35 U.S.C. § 103(a) as being unpatentable over: (1) Yu in view of Hopper and Avanzino; or (2) Yu in view of Hopper and Avanzino, and further in view of Chiang.

However, applicant nonetheless incorporates by reference herein, and maintains, applicant's related previous traversal within applicant's Amendment and Response filed 29 May 2002. Applicant's previous traversal was predicated upon applicant's assertion that Hopper does not disclose a dual damascene method employing a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, which provides an intrinsic etch stop within a dual damascene method with respect to anisotropic patterning of a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant less than about 4.0.

In that regard, applicant notes that all of the low dielectric constant materials disclosed by Hopper col. 3, lines 47-55 are carbon containing low dielectric constant dielectric materials which Hopper within col. 2, last paragraph and col. 3, first two paragraphs discloses as each being seriously deteriorated or completely etched within an oxygen containing plasma. Since they are each deteriorated or etched within an oxygen containing plasma, applicant asserts that: (1) Hopper has not disclosed etch stop properties for any one of Hopper's low dielectric constant dielectric materials with respect to another of Hopper's low dielectric constant dielectric materials (i.e., each and every limitation within applicant's invention as disclosed and claimed within claim 1 and claim 8) (MPEP 2143, 2143.03); and (2) when substituted into Yu's invention

in a fashion as suggested by the Examiner, a pair comprising two different of Hopper's low dielectric constant dielectric materials would presumably render Yu unsuitable for Yu's intended purpose since a dual damascene aperture would not be formed when etching a blanket second dielectric layer formed of a second of Hopper's low dielectric constant dielectric materials with respect to a patterned first dielectric layer formed of a first of Hopper's low dielectric constant dielectric materials (i.e, there is neither any suggestion or motivation to modify or combine Yu with Hopper nor is there any likelihood of success that the combination of Yu and Hopper will provide an operable invention) (MPEP 2143, 2143.01, 2143.02).

For these reasons as originally advanced within applicant's Amendment and Response filed 29 May 2002, applicant continues to assert that: (1) applicant's claims 1-7 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino; and (2) applicant's claims 8-15 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Yu in view of Hopper and Avanzino, and further in view of Chiang.

Other Considerations

Applicant acknowledges the additional prior art of record cited by the Examiner but not employed in rejecting applicant's invention, including (1) Cheek et al. (U.S. Patent No. 5,935,766); and (2) Nguyen et al. (U.S. Patent No. 6,043,164), as generally pertinent to applicant's invention.

No fee is due as a result of this Response.

67,200-367
Serial Number 09/821,554

SUMMARY

Applicant's invention as disclosed and claimed within claim 1 and claim 8 is directed at least in part towards a method for forming a dual damascene aperture through a dielectric layer. Applicant's method employs a patterned first dielectric layer and a blanket second dielectric layer formed of a corresponding first dielectric material and second dielectric material each having a dielectric constant of less than about 4.0, where the first dielectric material serves as an intrinsic etch stop with respect to the second dielectric material. A pertinent prior art reference employed in rejecting applicant's claims to applicant's invention may not properly be employed in rejecting applicant's claims to applicant's invention insofar as the pertinent prior art reference teaches away from that which is disclosed and claimed by applicant.

CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

Randy W. Tung (Reg. No. 31,311)

838 West Long Lake Road - Suite 120
Bloomfield Hills, MI 48302
248-540-4040 (voice)
248-540-4035 (facsimile)

67,200-367
Serial Number 09/821,554

APPENDIX

COMPLETE COPY OF THE CLAIMS

(MARKED-UP WITH CURRENT REVISIONS)

1. A method for forming an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via; and

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

2. The method of claim 1 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

3. The method of claim 1 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

4. The method of claim 1 wherein there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.

5. The method of claim 1 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

6. The method of claim 1 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

7. The method of claim 1 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

8. A method for forming a patterned conductor layer within an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method; and

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer.

9. The method of claim 8 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

10. The method of claim 8 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

11. The method of claim 8 wherein there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.

12. The method of claim 8 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

13. The method of claim 8 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

14. The method of claim 8 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

15. The method of claim 8 wherein the contiguous patterned conductor interconnect and patterned conductor stud layer is formed within the aperture while employing a chemical mechanical polish (CMP) planarizing method.